Interfacing Audio and Video Converters to Blackfin Processors

Presented By:
David Katz
Senior Blackfin Applications Engineer
About this Module

- This presentation will familiarize the user with the principles behind connecting Blackfin processors to audio and video devices.

- Prerequisites: Basic working knowledge of audio and video fundamentals
Module Outline

- Overview of Blackfin A/V Connectivity
  - Connecting to Audio Converters
    - Applicable Blackfin Audio Peripherals
    - Examples of HW/SW connections to Blackfin
    - Interfacing Tips and Tricks
    - Available Audio Collateral on Blackfin
  - Connecting to Video Converters
    - Digital Video Refresher
    - Applicable Video Peripheral(s)
    - Examples of HW/SW connections to Blackfin
    - Interfacing Tips and Tricks
    - Available Video Collateral on Blackfin
- Conclusion
Basic A/V System Connections

Audio DAC

Blackfin Processor

Video DAC

Audio ADC

Video ADC

Microphone

Camera
Why is Blackfin well-suited for A/V applications?

- Multimedia-grade performance
  - High clock speeds
  - Flexible instruction set
- Powerful Connectivity and Data Handling Capabilities
  - DMA capabilities
  - Peripheral mix
- Scalability across and within applications
  - Dynamic Power Management
  - Wide Product Portfolio
Connecting to Audio Converters
Blackfin Audio Interface Usage

- **Two-Wire Interface (TWI) and Serial Peripheral Interface (SPI)**
  - Forward channel used to configure and control audio converters
  - Reverse channel relays feedback info from converters

- **SPORT**
  - Used as data channel for audio data
    - SPORT TX connects to audio DAC
    - SPORT RX connects to audio ADC
    - Full-duplex SPORT RX/TX connects to audio codec

- In some codecs (e.g., AC97), SPORT also can serve as the codec control channel
**SPI Control Interface**

- Compatible with Motorola SPI standard
- Full-duplex serial interface operating up to 33 Mbps
- Supports Master/Slave and Multimaster environments
- 3-pin communication interface
  - MOSI = Master Output, Slave Input
  - MISO = Master Input, Slave Output
  - SCK = Serial Clock
- **SPISS = SPI Chip Select Input**
  - Allows another SPI device (Master) to select the processor (Slave)
- **SPISELx = SPI Slave Selects**
  - Allow the processor (Master) to select other SPI devices (Slaves)
TWI Control Interface

- I²C-compatible Two-Wire Interface
- Provides simple exchange method of control & data between multiple devices
- Simultaneous Master and Slave operation
- Supports speeds up to 400 kbits/sec
- SCL (clock) and SDA (data) pins comprise the interface

Source: Philips I²C Spec
SPORT: High-speed synchronous serial port

- Fully independent RX and TX channels
- Primary and secondary data RX/TX pins
- Operates up to 66 Mbps (133 Mbps including secondary RX/TX channel)
- Supports word lengths of 3-32 bits
- Programmable internal/external clocks and frame syncs
- Built-in hardware μ-Law and A-Law companding (for vocoders)
- Support for multichannel (TDM) interfaces for networked communication
- I²S signaling support

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DTxPRI</td>
<td>Transmit Data Primary</td>
</tr>
<tr>
<td>DTxSEC</td>
<td>Transmit Data Secondary</td>
</tr>
<tr>
<td>TSCLKx</td>
<td>Transmit Clock</td>
</tr>
<tr>
<td>TFSx</td>
<td>Transmit Frame Sync</td>
</tr>
<tr>
<td>DRxPRI</td>
<td>Receive Data Primary</td>
</tr>
<tr>
<td>DRxSEC</td>
<td>Receive Data Secondary</td>
</tr>
<tr>
<td>RSCLKx</td>
<td>Receive Clock</td>
</tr>
<tr>
<td>RFSx</td>
<td>Receive Frame Sync</td>
</tr>
</tbody>
</table>
SPORT I²S Functionality

- Industry standard developed by Philips for stereo audio transmission over a 3-wire interface
- Data always transmits in MSB format
- Consists of Serial Clock, Word Select (Left/Right) and Data
- Each SPORT accommodates 4 TX and 4 RX I²S audio channels
Connecting to Audio ADCs: AD1871
Connecting to Audio DACs: AD1854
**Tips & Tricks for Connecting to Audio Converters**

- **TWI**
  - Both SCL and SDA need pullup resistors; they are never driven high (per I²C spec)

- **SPI**
  - Connect all MISO pins to MISO pins, and MOSI to MOSI
  - Tie all MOSI pins together; tie all MISO pins together
  - Make sure MOSI and MISO pins are not swapped

- **SPORT**
  - SPORTs in Multi-Channel Mode that master the clocks and frame syncs should not connect TFS to RFS.
    - In this mode, the TFS frames the active TX channel data, acting as a TX Data Valid (TDV) pin.
  - Use proper termination for clock and frame sync signals
Additional Collateral for Audio Development

**Software**
- **VisualDSP++ Tools Suite**
  - Includes peripheral drivers for configuration via standard API
  - Includes complete audio device drivers
    - Standard API for audio converters, with many devices supported
      - AD1871 ADC
      - AD1854 DAC
      - AD1836A codec
- **EZ-Kit and EZ-Extender Card code examples**
  - Integrate peripheral and codec drivers
  - Provide examples of data flows and system configuration

**Hardware**
- **EZ-Kits + EZ-Extender Cards include on-board audio converters**
  - Allow for quick system prototyping
  - Reference Schematics and BOMs available

**VisualAudio® algorithm development tool**
- Streamlines design of audio systems
Connecting to Video Converters
 Outline for Connecting to Video Converters

- System Video Flow
- Some Digital Video Basics
  - ITU-R BT.601
  - ITU-R BT.656
- Blackfin Parallel Peripheral Interface (PPI)
- Connecting to Video Sources
- Connecting to Video Displays
- Sample Video System Diagram
System Video Flow

Video Sources
- Digital CMOS sensor
- Analog video camera or CCD
- Storage media
- Network

Outside World
- HW Decoder (A/D converter)

Video Displays
- TV or Monitor
- HW Encoder (D/A converter)

Blackfin Processor
- Enhancement/Analysis/Compression
- Uncompression/Formatting

Digital LCD panel
Digital Video Refresher
ITU-R BT.601 Concepts

- Specifies encoding parameters for digital TV

- Color Spaces Supported
  - RGB (Red, Green, Blue)
    - Intuitive format, but channels are highly correlated
    - 3 color values per pixel
      - RGB888 format implies 8 bits each of Red, Green and Blue
      - RGB666 or RGB565 imply 5 or 6 bits per color channel
  - YCbCr (Y=luma, Cx=chroma)
    - Generated via RGB signals
    - Highly uncorrelated, thus providing better compression characteristics
    - 4:2:2 YCbCr is recommended by BT.601
      - One luma and one chroma (Cr or Cb) value per pixel

- 8-bit or 10-bit quantization of RGB or YCbCr components

- NTSC and PAL normalized to 720 active pixels per line
  - NTSC (60 fields/sec) has 525 lines (including blanking)
  - PAL (50 fields/sec) has 625 lines (including blanking)
ITU-R BT.601 Timing

- **HSYNC** is the horizontal synchronization signal. It demarcates the start of active video on each row (left to right) of a video frame.

- **VSYNC** is the vertical synchronization signal. It defines the start (top to bottom) of a new video image.

- **FIELD** distinguishes, for interlaced video, which field (odd or even) of a video frame is currently being displayed. This signal is not applicable for progressive-scan video systems.

- **CLOCK** is the data clock for each pixel component.
ITU-R BT.656 Concepts

- Defines the physical interfaces and data streams necessary to implement ITU-R BT.601
- Bit-parallel and bit-serial modes
- 27 MHz nominal clock and 8 or 10 data lines (for bit-parallel mode)
- Embedded hardware signaling (H, V, F)
- Supports interlaced and progressive formats
ITU-R BT.656 NTSC and PAL Frames

NTSC

PAL
ITU-R BT.656 Data Stream Format

End of Active Video

- EAV Code (H=1)
  - FF 00 00 AB 80 10 80 10

- Horizontal Blanking
  - 80 10 FF 00 00

- SAV Code (H=0)
  - AB Cr Y Y Y Y Cr Y Y

Start of Active Video

Start of Next Line

Digital Video Stream

4 268 (280 for PAL) 4 1440

1716 (1728 for PAL)

AB = Control Byte
Blackfin Video Interface: PPI
Parallel Peripheral Interface

- Supports ITU-R BT.656 and BT.601 Video Converter Interfaces
- General-Purpose Mode supports data converter apps
Parallel Peripheral Interface

- Bidirectional, half-duplex interface
- Supports bit-parallel ITU-R BT.656 recommendation
- Up to 16 data lines, 1 clock, 3 Frame Syncs
- Programmable signal polarity choices for syncs and clock

Bandwidth-saving features
- Selective reception of BT.656 Active and Blanking regions
- Can optionally ignore Field 2 of a BT.656 frame
- Can skip even or odd data elements
- Works hand-in-hand with 2D DMA Engine
Connecting to Video Sources
Connecting to CMOS Image Sensors

- **Blackfin Processor**
  - PPI_FS1
  - PPI_FS2
  - PPI_CLK
- **Pixel Data[7:0]**
- **CMOS Imager**
- **Master Clock**
- **HSYNC (Line Valid)**
- **VSYNC (Frame Valid)**
- **Pixel Clock**
- **I²C Control Bus**
- **Serial Clock (SCK)**
- **Serial Data (SDA)**
Connecting to CMOS Image Sensors

- Blackfin EZ-Extender cards and EZ-Kits support connection to products from many major vendors
  - Micron
  - Omnivision
  - Kodak

- Example: Micron’s CMOS Imager “Headboard” provides a common 26-pin interface for a whole family of sensors
Connecting to Analog Sources: ADV7183B Video ADC
Connecting to Video Displays
Connecting to Analog Displays: ADV7174/ADV7179 Video DAC
Connecting to Digital TFT-LCD Panels
Tips and Tricks for Connecting to Video Devices

- Use ITU-R BT.656 mode whenever possible
  - Eliminates timing incongruities in sync modes

- Pay close attention to default converter settings

- Make sure clock source is as clean as possible

- For RGB565 connections, do not ground the LSB of R or B

  - Instead, tie the MSB of Red to the LSB of Red at the LCD panel
  - Do the same for Blue
  - This insures a full dynamic range is achievable on R and B channels
Additional Collateral for Video Development

**Software**
- **VisualDSP++ Tools Suite**
  - Includes peripheral drivers for configuration via standard API
  - Includes many complete video device drivers
    - ADV7183B
    - ADV7171, ADV7174, ADV7179
    - CMOS Sensors from Micron, Kodak and Omnivision
    - LCD displays from multiple vendors
- **EZ-Kit and EZ-Extender Card code examples**
  - Integrate peripheral and codec drivers
  - Provide examples of data flows and system configuration

**Hardware**
- **EZ-Kits + EZ-Extender Cards**
  - Include CMOS sensor and LCD panel interfaces
  - Allow for quick system prototyping
  - Reference Schematics and BOMs available
Video System Example

**Video Pass-Through**

1. **ADV7183B**
2. **BF561 (MJPEG Encoder)**
3. **ADV7179**
4. **USB NET2272**
5. **EZ-USB EXTENDER**
6. **ADSP-BF561 EZ-KIT**

- **Stack EZ-USB Extender onto ADSP-BF561 EZ-KIT**
- **USB 2.0 to Host PC**
  - Compressed Video flows from Blackfin to Host PC
  - *.AVI files get stored to local hard drive
Conclusion

- The Blackfin Processor architecture is very well suited for multimedia system design
- Blackfin devices provide versatile connectivity to A/V peripherals
- Collateral available to speed system design
Additional Information

- **Collateral to jump-start development**
  - VisualDSP++ tools suite for Blackfin Processors
    [www.analog.com/blackfin/visualdsp](http://www.analog.com/blackfin/visualdsp)
  - Blackfin EZ Kits and EZ-Extender Cards
    [www.analog.com/evaluationkits](http://www.analog.com/evaluationkits)
  - Application Notes
    [www.analog.com/ee-notes](http://www.analog.com/ee-notes)
  - BOLD online training modules
    [www.analog.com/BOLD](http://www.analog.com/BOLD)
  - VisualAudio® algorithm development tool
    [www.analog.com/visualaudio](http://www.analog.com/visualaudio)
  - Embedded Media Processing book
    [www.theEMPbook.com](http://www.theEMPbook.com)

- **Click “Ask A Question” button**
  Or send an email to [Processor.support@analog.com](mailto:Processor.support@analog.com)